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IEEE JNL IEEE Journal or Magazine

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 Liao, S.; Niou, C.; Chien, K.; Guo, A.; Dong, W.; Huang, C.;
[Reliability Physics Symposium Proceedings, 2003. 41st Annual. 2003 IEEE International 30 March-4 April 2003 Page\(s\):92 - 98](#)
 Digital Object Identifier 10.1109/RELPHY.2003.1197726
[AbstractPlus](#) | Full Text: [PDF\(454 KB\)](#) IEEE CNF
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- ☒ 2. **Novel test structures for the investigation of the efficiency of guard rings used for I/O-latch-up prevention**
 Quincke, J.;
[Microelectronic Test Structures, 1990. ICMTS 1990. Proceedings of the 1990 International Conference on 5-7 March 1990 Page\(s\):35 - 39](#)
 Digital Object Identifier 10.1109/ICMTS.1990.67876
[AbstractPlus](#) | Full Text: [PDF\(256 KB\)](#) IEEE CNF
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- ☐ 3. **psub guard ring design and modeling for the purpose of substrate noise isolation in the SOC era**
 Tsun-Lai Hsu; Yu-Chia Chen; Hua-Chou Tseng; Liang, V.; Jan, J.S.;
[Electron Device Letters, IEEE Volume 26, Issue 9, Sept. 2005 Page\(s\):693 - 695](#)
 Digital Object Identifier 10.1109/LED.2005.854351
[AbstractPlus](#) | Full Text: [PDF\(288 KB\)](#) IEEE JNL
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- ☐ 4. **Schottky barrier diodes with self-aligned floating guard rings**
 Chuang, C.T.; Arienzo, M.; Tang, D.D.; Isaac, R.;
[Electron Devices Meeting, 1983 International Volume 29, 1983 Page\(s\):666 - 669](#)
[AbstractPlus](#) | Full Text: [PDF\(304 KB\)](#) IEEE CNF
[Rights and Permissions](#)
- ☐ 5. **Design model and guidelines for n-well guard ring in epitaxial CMOS**
 Chih-Yao Huang; Ming-Jer Chen;
[Electron Devices, IEEE Transactions on Volume 41, Issue 10, Oct. 1994 Page\(s\):1806 - 1810](#)

Digital Object Identifier 10.1109/16.324585

[AbstractPlus](#) | Full Text: [PDF\(464 KB\)](#) IEEE JNL

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6. **Low-temperature characteristics of well-type guard rings in epitaxial CMOS**
Chih-Yao Huang; Ming-Jer Chen; Jeng-Kuo Jeng; Ching-Yuan Wu;
[Electron Devices, IEEE Transactions on](#)
Volume 43, Issue 12, Dec. 1996 Page(s):2249 - 2260
Digital Object Identifier 10.1109/16.544418
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(1444 KB\)](#) IEEE JNL
[Rights and Permissions](#)
7. **Improved latch-up immunity in junction-isolated smart power ICs with unbiased guard ring**
Gupta, S.; Beckman, J.C.; Kosier, S.L.;
[Electron Device Letters, IEEE](#)
Volume 22, Issue 12, Dec. 2001 Page(s):600 - 602
Digital Object Identifier 10.1109/55.974591
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(74 KB\)](#) IEEE JNL
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8. **Automatic methodology for placing the guard rings into chip layout to prevent latchup in CMOS IC's**
Ming-Dou Ker; Hsin-Chin Jiang; Jeng-Jie Peng; Tzay-Luen Shieh;
[Electronics, Circuits and Systems, 2001. ICECS 2001. The 8th IEEE International Conference on](#)
Volume 1, 2-5 Sept. 2001 Page(s):113 - 116 vol.1
Digital Object Identifier 10.1109/ICECS.2001.957690
[AbstractPlus](#) | Full Text: [PDF\(400 KB\)](#) IEEE CNF
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9. **A Schottky-barrier diode with self-aligned floating guard ring**
Chuang, C.T.; Arienzo, M.; Tang, D.D.-L.; Isaac, R.D.;
[Electron Devices, IEEE Transactions on](#)
Volume 31, Issue 10, Oct 1984 Page(s):1482 - 1486
[AbstractPlus](#) | Full Text: [PDF\(552 KB\)](#) IEEE JNL
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10. **Equivalent circuit modeling of guard ring structures for evaluation of substrate crosstalk isolation**
Kosaka, D.; Nagata, M.;
[Design Automation, 2006. Asia and South Pacific Conference on](#)
24-27 Jan. 2006 Page(s):6 pp.
Digital Object Identifier 10.1109/ASPDAC.2006.1594764
[AbstractPlus](#) | Full Text: [PDF\(558 KB\)](#) IEEE CNF
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11. **Suppression of avalanche multiplication at the periphery of diffused junction by floating guard rings in a planar InGaAs-InP avalanche photodiode**
Cho, S.R.; Yang, S.K.; Ma, J.S.; Lee, S.D.; Yu, J.S.; Choo, A.G.; Kim, T.I.; Burm, J.;
[Photonics Technology Letters, IEEE](#)
Volume 12, Issue 5, May 2000 Page(s):534 - 536
Digital Object Identifier 10.1109/68.841277
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(140 KB\)](#) IEEE JNL
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12. **Study of the correlation between the cutting edge current breakdown and the simulated lateral electrical field boundary in high resistivity silicon detectors with multi-guard ring structure**
Li, Z.; Huang, W.; Zhao, L.J.;